



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/727,612      | 12/05/2003  | Yukinori Akamine     | NITT-164            | 7467             |

38327 7590 11/27/2006

REED SMITH LLP  
3110 FAIRVIEW PARK DRIVE, SUITE 1400  
FALLS CHURCH, VA 22042

|          |
|----------|
| EXAMINER |
|----------|

VO, NGUYEN THANH

|          |              |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2618

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/727,612

Applicant(s)

AKAMINE ET AL.

Examiner

Nguyen T. Vo

Art Unit

2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 13 is/are rejected.
- 7) ☒ Claim(s) 9-12 and 14-20 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

1. The drawings were received on 9/20/2006. These drawings are acceptable.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacNally (US 6,516,185 B1, cited by examiner) in view of Herdey (US 2003/0098734, cited by examiner).

As to claim 1, MacNally discloses a direct conversion receiver (see figure 2) comprising a pair of mixers (see block 200 in figure 2; mixers 306 and 308 in figure 3) which convert a receive signal frequency (see the RF signal 201 in figure 2) to a

Art Unit: 2618

baseband frequency (see column 4 lines 61-64); and a baseband frequency signal processing block including a pair of first amplifiers (see filter/amplifiers 204 in figure 2) and a pair of first filters (see filter/amplifiers 204 in figure 2), following said mixers, wherein said baseband frequency signal processing block further includes a pair of negative feedback circuits (see the negative feedback circuit in figure 2) with adjustable feedback factor (see the adjustable offset integrator 206 in figure 2). MacNally thus discloses all the claimed limitations except that each negative feedback circuit includes a second filter of low-pass type, as recited in the claim. Herdey discloses in figure 1 a negative feedback circuit for reducing the DC offset (see numerals 106, 108 and 110), wherein the negative feedback circuit includes an adjustable feedback factor (see the **switched** capacitor integrator 108 in figure 4; paragraphs [0014], [0016], [0026]-[0031]), and a second filter of low-pass type (see the low pass filter 110). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above teaching of Herdey to MacNally, in order to benefit the advantages of Herdey's invention such as the switching frequency is proportional to the output signal thereby having the characteristics of a pseudo-random signal, contrary to common switched capacitors which generates undesirable noise (as suggested by Herdey at paragraph [0033]), and reduce DC offset (as suggested by Herdey at paragraph [0001]).

Regarding claim 2, the combination of MacNally and Herdey discloses that each negative feedback circuit comprises a second amplifier 412 (see Herdey, figure 4; paragraph [0027]) and said second filter 110 located following an output end of the second amplifier 412 as specified in the claim.

Regarding claim 3, the combination of MacNally and Herdey fails to disclose that the amplifier 412 (see figure 4 in Herdey) is a gain control amplifier as claimed. The examiner, however, takes Official Notice that such a gain control amplifier is known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above conventional gain control amplifier to the combination of MacNally and Herdey, in order to greatly reduce the DC offset in the direct conversion receiver.

Regarding claim 4, the combination of MacNally and Herdey fails to disclose that the low-pass filter 110 (see figure 1 in Herdey) is provided with an adjustable cut-off frequency as claimed. The examiner, however, takes Official Notice that such an adjustable cut-off frequency low-pass filter is known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above conventional adjustable cut-off frequency low-pass filter to the combination of MacNally and Herdey, in order to greatly reduce the DC offset in the direct conversion receiver.

5. Claims 5-8, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacNally in view of Herdey as applied to claim 1 above, and further in view of the prior art as admitted by applicant in figure 5 of the present application.

As to claims 5-8, the combination of MacNally and Herdey fails to disclose a pair of DC offset cancellation circuit as claimed. The prior art of figure 5 discloses a pair of DC offset cancellation circuit, each comprising an analog to digital converter (see the ADC) which is connected to an output of one of said pair of first amplifiers 104 to

Art Unit: 2618

convert analog signals to digital signals; a digital processing circuit CTL which detects a DC offset voltage out of output signals from said analog to digital converter and calculates a voltage to cancel the DC offset voltage; and a digital to analog converter DAC which converts a digital signal of the voltage calculated by the digital processing circuit into an analog signal of the voltage and supplies the analog signal of the voltage to said one of said pair of first amplifiers. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the above teaching of the prior art of figure 5 to the above combination of McNally and Herdey, in order to further reduce the DC offset in the direct conversion receiver.

As to claim 13, first of all the rejection to claims 5-8 is herein incorporated. In addition, the admitted prior art of figure 5 further discloses multistage compositions of amplifiers (see multistage 104 in figure 5).

***Allowable Subject Matter***

6. Claims 9-12, 14-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 9-12, 14, the applied references fail to disclose or render obvious that the direct conversion receiver performs DC offset cancellation by means of said pair of DC offset cancellation circuits when being powered on and, subsequently, performs DC offset cancellation by means of said pair of negative feedback circuits, as specified in the claim.

Art Unit: 2618

As to claims 15-17, the applied references fail to disclose or render obvious that each of said pair of first amplifiers is made up of multiple stages of gain control amplifiers and a last-stage static gain amplifier and each said negative feedback circuit loops back to an output of a first stage gain control amplifier, as specified in the claims.

As to claims 18-20, the applied references fail to disclose or render obvious that said pair of first amplifiers are pair of gain control amplifiers having circuitry in which a plurality of different resistance elements are located so as to connect to a common terminal of the emitter side of a couple of differential transistors and gain is changed in steps by switching on/off current flowing through the plurality of resistance elements, as specified in the claims.

### ***Response to Arguments***

7. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ruelke (US 6,459,889 B1) and Shi (US 7,136,431 B2) all disclose direct conversion receivers.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2618

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Vo whose telephone number is (571) 272-7901. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571)272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 2618

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nguyen Vo

*Nguyen Vo*  
11-16-2006

**NGUYENT.VO**  
**PRIMARY EXAMINER**